PTO/SB/33 (07-05)
Approved for use through xx/xx/200x. OMB 0651-00xx
U.S. Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE

PRE-APPEAL BRIEF REQUEST FOR REVIEW		Docket Number: 07977-088902
I hereby certify under 37 CFR §1.8(a) that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to Mail Stop AF, Commissioner for Patents, Box 1450, Alexandria, VA 22313-1450.	Application Number: 09/362,808	Filed: July 28, 1999
	First Named Inventor: Hongyong Zhang	
Date of Deposit	Art Unit: 2814	Examiner: Shrinivas H. Rao
Signature		
Typed or Printed Name of Person Signing Certificate		

Applicant requests review of the final rejection in the above-identified application. No amendments are being filed with this request.

This request is being filed with a Notice of Appeal.

The review is requested for the reason(s) stated on the attached sheet(s).
Note: No more than five (5) pages may be provided.

I am the

☐ applicant/inventor.

☐ assignee of record of the entire interest.
See 37 CFR 3.71. Statement under 37 CFR 3.73(b) is enclosed. (Form PTO/SB/96)

☒ attorney or agent of record 37,640 (Reg. No.)

☐ attorney or agent acting under 37 CFR 1.34.
Registration number if acting under 37 CFR 1.34 _____

Signature

John P. Hayden
Typed or printed name

(202) 783-5070
Telephone number

November 6, 2006
Date

NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more than one signature is required, see below.

☒ Total of 5 forms are submitted.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant	: Hongyong Zhang	Art Unit	: 2814
Serial No.	: 09/362,808	Examiner	: Shrinivas H. Rao
Filed	: July 28, 1999	Conf. No.	: 7320
Title	: METHOD OF FABRICATING SEMICONDUCTOR DEVICE		

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

PRE-APPEAL BRIEF REQUEST FOR REVIEW

Pursuant to United States Patent and Trademark Office OG Notices: 12 July 2005 - New Pre-Appeal Brief Conference Pilot Program, a request for a review of identified matters on appeal is hereby submitted with the Notice of Appeal. Review of these identified matters by a panel of examiners is requested because the rejections of record are clearly not proper and are without basis, in view of a clear legal or factual deficiency in the rejections. All rights to address additional matters on appeal in any subsequent appeal brief are hereby reserved.

Claims 1-49 are currently pending, with claims 1, 6, 10, 14, 19, 24, 44 and 47 being independent. Claims 1-13, 33 and 34 are allowed. Claims 14-30, 35-37 and 41-49 have been rejected as being unpatentable over Fu in view of Sasaki and Lin.

Applicant specifically asks the panel to review the issues highlighted below.

Neither Fu, Sasaki, Lin, nor any proper combination of the three describes or suggests a first interlayer insulating film having a smaller taper angle and over an insulating film and a gate electrode, and a second interlayer insulating film having a larger taper angle and over the first interlayer insulating film, as recited in claims 14, 19, 44 and 47.

Claim 14 is directed to a semiconductor device that includes a semiconductor layer formed over a substrate having an insulating surface and including at least channel, source and drain regions, an insulating film on the semiconductor layer, a gate electrode over the insulating film, a first interlayer insulating film over the insulating film and over the gate electrode, and a second interlayer insulating film over the first interlayer insulating film. The device also

includes at least one contact hole having a tapered section and formed in the first and second interlayer insulating films and the insulating film, and an electrode formed on the contact hole and connected with one of the source and drain regions through the contact hole. Claim 14 further recites that ***a taper angle β of an inner surface of the second interlayer insulating film in the contact hole with respect to a major surface of the semiconductor layer is larger than a taper angle α of an inner surface of the first interlayer insulating film in the contact hole with respect to the major surface of the semiconductor layer.***

The current office action provides two different explanations as to how Lin is believed to describe the recited arrangement of taper angles. First, in the body of the rejection, the action appears to indicate that the layers 16/18 of Lin together have the recited larger taper angle β, and that the layers 20/22 together have the recited smaller taper angle α. Second, in the response to arguments section, the action appears to argue that one of the layers 16/18 has the recited larger taper angle β and the other has the recited taper angle α, or that one of the layers 20/22 has the recited larger taper angle β and the other has the recited taper angle α. In addition, at an interview, the Examiner indicated that claim 14 does not presently include language that prevents the claim from reading on the arrangement of Lin. Applicant respectfully disagrees.

As shown above, claim 14 requires the second interlayer insulating film to be over the first interlayer insulating film, and further requires the first interlayer insulating film to be over the insulating film and the gate electrode (which, in turn, are over the semiconductor layer formed over the substrate). Thus, according to claim 14, the first interlayer insulating film (which has the smaller taper angle) is between the substrate and the second interlayer insulating film (which has the larger taper angle).

With reference to Fig. 6 of Lin, if the layer 16 of Lin is said to correspond to the recited first interlayer insulating film, the layer 18 could not qualify as the second interlayer insulating film because the layers 16 and 18 have the same taper angle. Nor could either of the layers 20 and 22 qualify, since both of these layers have a smaller taper angle than layer 16, which is located between these layers and the substrate, while the claim requires a larger taper angle.

If the layer 18 of Lin is said to correspond to the recited first interlayer insulating film, the layer 16 could not qualify as the second interlayer insulating film because the layer 18 is not between the layer 16 and the substrate, and because the layers 16 and 18 have the same taper

angle. Nor could either of the layers 20 and 22 qualify, since both of these layers have a smaller taper angle than the layer 18, which is located between these layers and the substrate, while the claim requires a larger taper angle.

If the layer 20 of Lin is said to correspond to the recited first interlayer insulating film, neither of the layers 16 and 18 could qualify as the second interlayer insulating film because claim 20 is not between either of the layers 16 and 18 and the substrate. The layer 22 also could not qualify as the second interlayer insulating film because the layers 20 and 22 have the same taper angle.

If the layer 22 of Lin is said to correspond to the recited first interlayer insulating film, none of the layers 16, 18 and 20 could qualify as the second interlayer insulating film because the layer 22 is not between any of the layers 16, 18 and 20 and the substrate.

Accordingly, since no possible combination of the layers 16-20 of Lin satisfy the relationship set forth in claim 14, Lin does not satisfy this relationship and the rejection of claim 14 and its dependent claims should be withdrawn.

Like claim 14, each of independent claims 19, 44 and 47 recites an arrangement in which a first insulating film (which has the smaller taper angle) is between a substrate and a second insulating film (which has the larger taper angle). Accordingly the rejection of claims 19, 44 and 47, along with their dependent claims, should be withdrawn for the reasons discussed above with respect to claim 14.

Neither Fu, Sasaki, Lin, nor any proper combination of the three describes or suggests a semiconductor layer formed over a substrate having an insulating surface and having a channel region, at least one low doped impurity region, and at least one high doped impurity region that is adjacent to the channel region with the low doped impurity region interposed therebetween, as recited in claim 24.

As best understood, the rejection asserts that Fig. 2e of Sasaki shows this feature with the regions 15, 16 being the low doped impurity regions and the regions 15', 16' being the high doped impurity regions, and the region between the regions 15, 16 being the channel region. However, in Sasaki, the regions 15, 16, 15' and 16' are formed in the substrate 11. As such,

Sasaki does not describe or suggest the semiconductor layer recited in claim 24. Nor does there appear to be any motivation to combine Fu, Sasaki and Lin to somehow arrive at this feature. Accordingly, the rejection of claim 24 and its dependent claims should be withdrawn.

Applicant submits that all claims are in condition for allowance.

Please apply any other charges or credits to Deposit Account No. 06-1050.

Respectfully submitted,

Date: 11/6/06

John F. Hayden
Reg. No. 37,640

Fish & Richardson P.C.
1425 K Street, N.W.
11th Floor
Washington, DC 20005-3500
Telephone: (202) 783-5070
Facsimile: (202) 783-2331

40377624.doc